ABSTRACT OF THE DISCLOSURE

A receiver apparatus having a demodulator circuit that demodulates transmitted serial data into parallel data by sampling the transmitted serial data on the basis of a first and a second clock signals having different numbers of clocks to be output in synchronization with a cycle of a transmitted clock includes a first synchronizing circuit that generates the first clock signal synchronized with the cycle of the transmitted clock, and a second synchronizing circuit that generates the second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from the first clock signal. The demodulator circuit comprises the second synchronizing circuit, a sampling register that samples the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit that calculates a difference relative to the input clock signal of the transmitted serial data on the basis of a sampled data sampled by the sampling register, and a clock select circuit that adjusts a phase of a symbol-sampled signal on the basis of the difference.